Remarks

Claims 38 – 112 are pending. Applicant now responds to the Examiner's objections and rejections as set out paragraph by paragraph in the Office Action.

¶4: The Abstract has been amended to better summarize the invention. Thus, applicant believes that the objection to the specification has been overcome at this time.

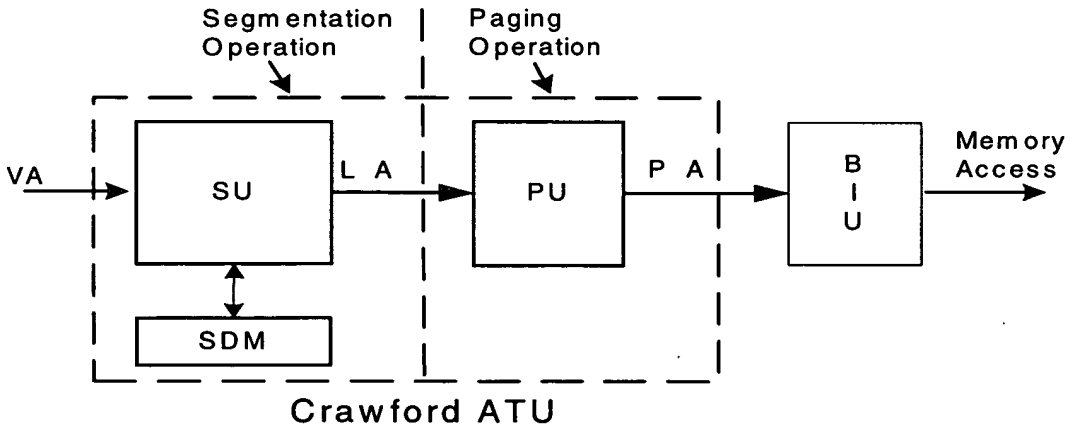
¶5: Claim 38 has been amended. As presently structured, this claim is believed to overcome the Examiner's rejection under § 112 for overbreadth. Claims 39, 41, and 42 depend from claim 38, and thus the present amendment should remove the objections for these claims as well.

¶6 – 7 : Claims 1 – 5 have been canceled without waiver or prejudice. This should obviate the double patenting rejection under § 101.

The following comments are provided in response to the Examiner's rejections of the claims under § 103 in ¶ 8 – 12 of the Office Action.

THE BASIC STRUCTURAL AND OPERATIONAL FEATURES OF THE PRIOR ART AND THE APPLICANT'S INVENTION

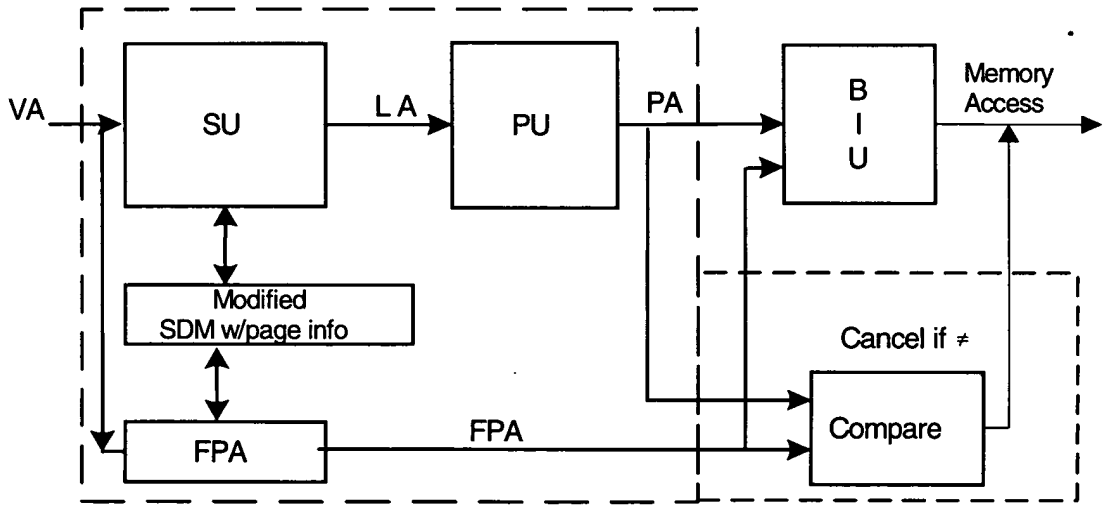
To facilitate the present discussion, applicants have generated the following simplified block diagram of the Crawford '836 reference relied upon by the Examiner, as well as a corresponding simplified block diagram of the present invention:



The Examiner acknowledges that Crawford '836 does not disclose anything which generates either a "fast" physical address, or a "tentative" or "speculative" memory reference. This is a key and important distinction, because the terms "fast," "tentative" and "speculative" have a plain meaning which is entirely incompatible with the type of structure used by Crawford '836 to generate

physical addresses. Moreover, the Toy reference would not teach one of skill in the art to modify Crawford '836 in any fashion, because the latter specifically teaches away from such modifications as explained below.

The operation of the Crawford reference is demonstrable from the above diagram. Looking at the Crawford '836 Address Translation Unit (ATU) approach, each Virtual Address (VA) is converted by a segmentation unit (SU) during a first operation into a Linear Address (LA) using information from a segment descriptor memory (SDM). The LA is then in turn converted into a Physical address (PA) by a paging unit (PU) in a second operation and then used by a bus interface unit (BIU) to initiate a memory access. This set of operations takes place in the same slow, sequential manner for *every* virtual address, with no regard given to any characteristics of such address, prior address information, etc. It is always a two step operation, and, for each translation, takes the same exact time to complete; therefore it is inefficient in most cases.



Applicant's ATU

Looking at the applicants' claimed invention, in an Address Translation Unit (ATU) approach, after a first virtual address is converted, the physical address information from such conversion is kept in a modified segment descriptor memory, accessed by segment identifier, which supplies this information to a fast physical address generator. Thereafter, each subsequent Virtual Address (VA) whose segment identifier is the same is converted by a fast physical address generator to create a tentative or speculative address used by a bus interface unit (BIU) to initiate a memory access. In other words, this memory access is initiated extremely rapidly, without waiting for the two-step translation noted above to complete. The *only* time the two-step calculated physical

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address is used to access memory is when a portion of such calculated physical address is different from the corresponding portion of the tentative or speculative address. When the two portions are different, the tentative memory access is discontinued by the comparator, and a memory access based on the fully calculated physical address is instead performed.

From the above-simplified pictures and description, is readily apparent how the applicant's claims distinguish over Crawford and the prior art. The modified segment descriptor memory claimed herein, therefore, is quite important, and serves to provide the present invention with functionality (rapid address translation) unavailable in the Crawford type approach. Crawford does not have anything remotely resembling the structure used in the applicant's claimed inventions for storing physical address information in a segment descriptor memory. Nor does it generate tentative or speculative addresses or memory references. There is no mechanism or suggestion for computing a physical address faster from one virtual address to the next. There is no teaching or suggestion for having both fast physical address and a regular address computed at the same time, or in parallel. None of these teachings exist because the Crawford type approach, with strict separation of segmentation and paging, cannot achieve such functionality.

GENERAL DISCUSSION OF PRESENT REJECTIONS

The Examiner nonetheless asserts in ¶ 12 of the Office Action that it is "obvious" to modify Crawford '836 based on the Toy reference to arrive at the applicant's claimed inventions. As the Examiner is well aware nonetheless, for this rejection to be sustainable, there must be some suggestion, teaching, or motivation in Crawford '836, Toy, or some other prior art reference, to perform this modification. And yet, the Examiner *acknowledges* that such information is not to be found in Crawford '836, Toy, or anyplace else for that matter. Crawford nowhere mentions anything except the standard sequential logical-linear-physical calculation for a memory reference. Toy contains no mention or suggestion that the scheme shown therein (which the Examiner acknowledges is "non segmented"[1]) can be applied to a segmented operating system, and more importantly, does not explain how this would be done. Non-segmented address systems are addressed at length in the background of the present disclosure; they are not relevant to the present invention, in large part because they are not subject to the same constraints as a segment plus optional paging type address system as shown in Crawford. It is not surprising, therefore, that Toy

[1] While the Toy reference mentions a "segment" as part of the virtual address, this is clearly a different kind of segment than that discussed by Crawford. This is apparent from the fact that there is no segment ID or segment offset in the virtual address, and by the fact that the virtual address in Toy is never converted to a linear address. Instead the virtual address, which contains paging information, is merely converted in one step to a physical address, which is unlike the virtual-linear-physical type approach disclosed in Crawford.

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contains no suggestion for implementing the scheme shown there within an operating system that utilizes separate segment + paging operations.

On this basis alone Applicants submit that the present rejections are improper under applicable case law interpreting § 103, and must be withdrawn. *See e.g, In Re Bond, 15 U.S.P.Q. 2d 1566, 1568-69* (Fed. Cir. 1990) ("obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination."); *In Re Gordon, 221 U.S.P.Q. 1125 (Fed. Cir. 1984)* ("The mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification")

The cases are quite clear that the Examiner cannot simply make a bald, conclusory, unsupported statement about what one of skill in the art would find "obvious." *See e.g., In Re Fine, 5 U.S.P.Q. 2d 1596, 1599* (Fed. Cir. 1988) (Board's "bald assertion" that something was within the level of skill in the art is not sufficient evidence to support an obviousness finding). Yet in this case, there is no suggestion cited (and none exists) to support any argument that it might somehow be obvious to combine Crawford '836 with Toy to arrive at the claimed invention. This unsupported analysis suffers other problems: first, it relies on hindsight reconstruction; and second, the Toy reference ATU is *incompatible* with the type of ATU shown in Crawford. In system such as Toy, paging information, including physical address information, is contained within the virtual address. See e.g., the Toy reference at column 3:, ll. 57+ "The virtual address is composed of segment, page, and word address bits." The plain teachings of Crawford show that a virtual address (as well as any segment descriptor tables in a segmentation and optional paging environment) can contain no paging information, or physical address information. This would, in essence, combine segmentation and paging together, and the Crawford '836 reference itself explicitly teaches away from such combination. These facts, too, refute any insinuation that the claimed invention is obvious in light of the art.

IN REJECTING CLAIMS 37 - 81 THE EXAMINER IMPROPERLY MODIFIES CRAWFORD '836 IN A MANNER INCONSISTENT WITH THE TEACHINGS OF THAT REFERENCE

In ¶ 12 of the Office Action the Examiner relies on an argument that the ATU 20 in Crawford can be modified to include a speculative address generator as described in Toy. Yet, on its face, Crawford '836 is incompatible with the type of address translation logic shown in Toy, which, as mentioned above, uses paging information in the virtual address. Crawford cannot

handle virtual addresses having paging information, and cannot handle paging information during a segmentation operation. *See e.g.*, FIG. 2, the dotted line indicating the demarcation between a segmentation and paging unit. A quick review of the '836 claims confirms that paging information cannot be used during the first part of the address translation (from virtual to linear):

> "...said segment descriptor table describing segments *without reference to whether a segment is paged or unpaged.*" See claim 3, column 10, ll. 9 – 14 (emphasis added).

The other '836 claims have similar limitations requiring that there be *no* paging information in the segmentation descriptor memory, or in the segmentation unit during an address translation. This separation is also categorically enforced in the teachings of the specification, which notes:

> "Segments are defined by a set of segment descriptor tables that are *separate from the page tables* used to describe the page translation." *See* column 3, ll. 11 – 13 (emphasis added).

Thus, Crawford '836 explicitly discourages, and teaches away from, the use of any system, such as that shown in Toy, where segment and paging information is combined.

Applicant was the first to conceive and develop a viable mechanism that provides fast memory references in a segmentation plus optional paging system. There is simply no teaching, suggestion or hint in Toy (or elsewhere) about how to achieve such functionality in such environment. Accordingly, under these circumstances, there is compelling evidence that the claims are non-obvious, and should be allowed.

When a reference explicitly teaches away from the kind of modification proposed by the Examiner, a rejection for obviousness is not proper. *See In Re Fine, supra*, at 1599: "...instead of suggesting that the system be used to detect nitrogen compounds, Eads deliberately seeks to avoid them; it warns against rather than teaches Fine's invention." Similarly, in *In Re Gordon, supra*, 221 U.S.P.Q. at 112, the same conclusion was reached: "...if the French apparatus were turned upside down, it would be rendered inoperable for its intended purpose....[I]n effect, French teaches away from the board's proposed modification." It is crystal clear, from a plain reading of the Crawford reference, that it specifically and actively discourages the use of an address translation system such as shown in Toy, which includes paging information in the virtual address. Crawford is entirely incompatible with such approach, and does not indicate to one of skill in the art how to overcome such incompatibility. Using the virtual address system of Toy, including an accelerated address generated by using paging information, would in fact defeat the whole purpose of the very carefully set up separate segmentation/paging operations described in Crawford. Thus, the present rejections for obviousness should be withdrawn.

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There are other important limitations in the claims which the Examiner has also not addressed, or explained why they are obvious in light of the prior art, even if one of skill in the art were to modify Crawford to include the teachings of Toy. The latter, for example, mentions nothing about "linear" addresses, and yet such types of addresses are described in all of the pending claims. Many of the present claims mention the relative timing between the operational steps needed to compute an actual physical address and the operations used to create speculative or tentative memory addresses. Yet, the Toy reference teaches and suggests nothing about this aspect of the invention whatsoever. In large part this is because Toy, as indicated above, is not a virtual-linear-physical address translation system, and therefore does not (and cannot) teach anything to one of skill in the art about the desired timing relationship of such operations. Accordingly, this aspect of many of the claims is not obvious from any of the prior art. This includes claim 43 (which indicates generally that the tentative physical address is generated before the actual linear address is computed), claim 49 (which recites that fast physical addresses can be generated while virtual addresses are being converted into linear addresses), claim 57 (which indicates that a fast physical address for a second can be generated based on prior physical address information and the first linear address before computations for the first linear address have actually been completed); claim 70 (the tentative memory reference can be generated while virtual addresses are being converted into linear addresses. Many of the independent claims include similar limitations: *see, e.g.* claims 44 – 48; 50 – 53; 58 – 60; 64; 69; 70 – 73; 75; 81. This is yet another reason why the claims are distinguishable over the art.

NEWLY SUBMITTED CLAIMS 38 - 49 ARE PATENTABLE OVER CRAWFORD AS WELL

Newly submitted claims 81 - 111 are also believed to be patentable at this time for the reasons set forth above. For new claims 82 – 85, 89 – 94, and 107 – 112, as discussed above, Toy does not include any suggestion to modify the type of structure shown in Crawford to include a fast memory reference, and does not mention anything about "linear" addresses. This same argument applies with equal force to claims 86 – 88, and 95 – 100, 101 – 106; it is apparent, also, that Toy says nothing about a "segment identifier" or a "segment offset" as called for in these claims.

CONCLUSION

Consequently, the Examiner's present rejections require that one of skill in the art disregard the plain teachings of the Crawford '836 approach, and then radically modify the ATU shown there with the teachings of Toy to arrive at the claimed invention. This is not an acceptable basis for rejecting the claims under §103, especially since there is no suggestion in either Crawford or Toy to

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do so. As the Examiner may not have understood that this type of radical re-engineering of Crawford '836 might be necessary, applicants submit that the present rejections are not supportable.

The present invention therefore is structurally and operationally different from the standard address translation logic shown in Crawford '836. These differences result in a noticeable improvement over Crawford '836, by avoiding repetitive virtual-linear-physical address calculations in segmentation plus optional paging address translation systems. Accordingly, claims are distinguishable over the prior art, including Crawford '836 and Toy, and should be allowable.

A check in the amount of $ 513 has been enclosed to cover the costs of the newly filed claims (6 new independent claims ($39 each) and 31 new claims total ($9 each)).

Should the Examiner believe it that it would be helpful to discuss any of the above points in person, Applicant is open to a telephone conference (408-342-1862) at any convenient time.

These points and others are now discussed in detail.

Respectfully submitted,

Law+

Date: November 24, 1998

J. Nicholas Gross, Attorney, Reg. No. 34,175

I hereby certify that the foregoing is being deposited with the U.S. Postal Service, postage prepaid, to the Commissioner of Patents and Trademarks, this 24th day of November 1998.